IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Previously Presented) A camera comprising:

a display portion; and

a nonvolatile memory, the nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

a first circuit for electrically reading a threshold voltage of the memory transistor by using a threshold voltage of the reference memory transistor;

a second circuit for performing electrical write on the memory transistor until the threshold voltage of the memory transistor is higher than a first reference voltage; and

a third circuit for performing electrical write on the reference memory transistor until the threshold voltage of the reference memory transistor is higher than a second reference voltage.

2-90 (Canceled)

91. (Previously Presented) A camera according to claim 1, wherein the first reference voltage is higher than the second reference voltage.

92. (Previously Presented) A camera according to claim 1, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

93. (Previously Presented) A camera according to claim 1, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

94. (Previously Presented) A camera according to claim 1, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

95. (Previously Presented) A camera according to claim 1, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

96. (Previously Presented) A camera according to claim 1, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

97. (Previously Presented) A camera according to claim 1, wherein the memory transistor and the reference memory transistor store multilevel information.

98. (Previously Presented) A camera comprising:

a display portion; and

a nonvolatile memory, the nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

a first circuit for performing electrical write on the memory transistor until a first threshold voltage of the memory transistor, which is read based on a reference voltage of the reference memory transistor, and a second threshold voltage of the memory transistor, which is read based on a first reference voltage of the reference memory transistor belong to a distribution of threshold voltages for same information; and

a second circuit for performing electrical write on the reference memory transistor until a threshold voltage of the reference memory transistor is higher than a second reference voltage.

99. (Previously Presented) A camera according to claim 98, wherein the first reference voltage is higher than the second reference voltage.

100. (Previously Presented) A camera according to claim 98, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

101. (Previously Presented) A camera according to claim 98, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge

accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

102. (Previously Presented) A camera according to claim 98, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

103. (Previously Presented) A camera according to claim 98, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

104. (Previously Presented) A camera according to claim 98, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

105. (Previously Presented) A camera according to claim 98, wherein the memory transistor and the reference memory transistor store multilevel information.

106. (Previously Presented) A camera comprising:

a display portion; and

a nonvolatile memory, the nonvolatile memory comprising:

a unit cell in which multiple memory transistors are connected in series;

a reference memory transistor;

a first circuit for electrically reading a threshold voltage of the memory transistor by using a threshold voltage of the reference memory transistor;

a second circuit for performing electrical write on the memory transistor until the threshold voltage of the memory transistor is higher than a first reference voltage; and

a third circuit for performing electrical write on the reference memory transistor until the threshold voltage of the reference memory transistor is higher than a second reference voltage.

107. (Previously Presented) Á camera according to claim 106, wherein the first reference voltage is higher than the second reference voltage.

108. (Previously Presented) A camera according to claim 106, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

109. (Previously Presented) A camera according to claim 106, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

110. (Previously Presented) A camera according to claim 106, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating

gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

111. (Previously Presented) A camera according to claim 106, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

112. (Previously Presented) A camera according to claim 106, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

113. (Previously Presented) A camera according to claim 106, wherein the memory transistor and the reference memory transistor store multilevel information.

114. (Currently Amended) A camera comprising:

a display portion; and

a nonvolatile memory the nonvolatile memory comprising:

a unit cell in which multiple memory transistors are connected in series;

a reference memory transistor;

a first circuit for performing electrical write on the memory transistor until a first threshold voltage of the memory transistor, which is read from a reference voltage of the

reference memory transistor, and a second threshold voltage of the memory transistor, which is read from a first reference voltage of the reference memory transistor belong to a distribution of threshold voltages for same information; and

a second circuit for performing electrical write on the reference memory transistor until a threshold voltage of the reference memory transistor is higher than a second reference voltage.

115. (Previously Presented) A camera according to claim 114, wherein the first reference voltage is higher than the second reference voltage.

116. (Previously Presented) A camera according to claim 114, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

117. (Previously Presented) A camera according to claim 114, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

118. (Previously Presented) A camera according to claim 114, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

119. (Previously Presented) A camera according to claim 114, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

120. (Previously Presented) A camera according to claim 114, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

121. (Previously Presented) A camera according to claim 114, wherein the memory transistor and the reference memory transistor store multilevel information.

122. (Previously Presented) A camera comprising:

a display portion: and

a nonvolatile memory, the nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

a timer;

a first circuit for performing electrical write on the memory transistor for each time when an elapsed time measured by the timer reaches an arbitrarily preset time until a threshold voltage of the memory transistor, which is read based on a reference voltage of the reference memory transistor is higher than a first reference voltage; and

a second circuit for performing electrical write on the reference memory transistor until a threshold voltage of the reference memory transistor is higher than a second reference voltage.

123. (Previously Presented) A camera according to claim 122, wherein the first reference voltage is higher than the second reference voltage.

124. (Previously Presented) A camera according to claim 122, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

125. (Previously Presented) A camera according to claim 122, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

126. (Previously Presented) A camera according to claim 122, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

127. (Previously Presented) A camera according to claim 122, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

128. (Previously Presented) A camera according to claim 122, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

129. (Previously Presented) A camera according to claim 122, wherein the memory transistor and the reference memory transistor store multilevel information.

130. (Previously Presented) A mobile information terminal comprising:

a display portion; and

a nonvolatile memory, the nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

a first circuit for electrically reading a threshold voltage of the memory transistor by using a threshold voltage of the reference memory transistor;

a second circuit for performing electrical write on the memory transistor until the threshold voltage of the memory transistor is higher than a first reference voltage; and

a third circuit for performing electrical write on the reference memory transistor until the threshold voltage of the reference memory transistor is higher than a second reference voltage.

131. (Previously Presented) A mobile information terminal according to claim 130, wherein the first reference voltage is higher than the second reference voltage.

132. (Previously Presented) A mobile information terminal according to claim 130, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

133. (Previously Presented) A mobile information terminal according to claim 130, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

134. (Previously Presented) A mobile information terminal according to claim 130, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

135. (Previously Presented) A mobile information terminal according to claim 130, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

136. (Previously Presented) A mobile information terminal according to claim 130, wherein each of the memory transistor and the reference memory transistor comprises an active

region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

137. (Previously Presented) A mobile information terminal according to claim 130, wherein the memory transistor and the reference memory transistor store multilevel information.

138. (Previously Presented) A mobile information terminal comprising:

a display portion; and

a nonvolatile memory, the nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

a first circuit for performing electrical write on the memory transistor until a first threshold voltage of the memory transistor, which is read based on a reference voltage of the reference memory transistor, and a second threshold voltage of the memory transistor, which is read based on a first reference voltage of the reference memory transistor belong to a distribution of threshold voltages for same information; and

a second circuit for performing electrical write on the reference memory transistor until a threshold voltage of the reference memory transistor is higher than a second reference voltage.

139. (Previously Presented) A mobile information terminal according to claim 138, wherein the first reference voltage is higher than the second reference voltage.

140. (Previously Presented) A mobile information terminal according to claim 138, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

141. (Previously Presented) A mobile information terminal according to claim 138, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

142. (Previously Presented) A mobile information terminal according to claim 138, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

143. (Previously Presented) A mobile information terminal according to claim 138, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

144. (Previously Presented) A mobile information terminal according to claim 138, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

145. (Previously Presented) A mobile information terminal according to claim 138, wherein the memory transistor and the reference memory transistor store multilevel information.

146. (Previously Presented) A mobile information terminal comprising:

a display portion; and

a nonvolatile memory, the nonvolatile memory comprising:

a unit cell in which multiple memory transistors are connected in series;

a reference memory transistor;

a first circuit for electrically reading a threshold voltage of the memory transistor by using a threshold voltage of the reference memory transistor;

a second circuit for performing electrical write on the memory transistor until the threshold voltage of the memory transistor is higher than a first reference voltage; and

a third circuit for performing electrical write on the reference memory transistor until the threshold voltage of the reference memory transistor is higher than a second reference voltage.

147. (Previously Presented) A mobile information terminal according to claim 146, wherein the first reference voltage is higher than the second reference voltage.

148. (Previously Presented) A mobile information terminal according to claim 146, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

149. (Previously Presented) A mobile information terminal according to claim 146, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

150. (Previously Presented) A mobile information terminal according to claim 146, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

151. (Previously Presented) A mobile information terminal according to claim 146, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

152. (Previously Presented) A mobile information terminal according to claim 146, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

153. (Previously Presented) A mobile information terminal according to claim 146, wherein the memory transistor and the reference memory transistor store multilevel information.

154. (Previously Presented) A mobile information terminal comprising:

a display portion; and

a nonvolatile memory the nonvolatile memory comprising:

a unit cell in which multiple memory transistors are connected in series;

reference memory transistor;

a first circuit for performing electrical write on the memory transistor until a first threshold voltage of the memory transistor, which is read from a reference voltage of the reference memory transistor, and a second threshold voltage of the memory transistor, which is read from a first reference voltage of the reference memory transistor belong to a distribution of threshold voltages for same information; and

a second circuit for performing electrical write on the reference memory transistor until a threshold voltage of the reference memory transistor is higher than a second reference voltage.

155. (Previously Presented) A mobile information terminal a according to claim 154, wherein the first reference voltage is higher than the second reference voltage.

156. (Previously Presented) A mobile information terminal according to claim 154, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

157. (Previously Presented) A mobile information terminal according to claim 154, wherein each of the memory transistor and the reference memory transistor comprises an active

region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

158. (Previously Presented) A mobile information terminal a according to claim 154, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

159. (Previously Presented) A mobile information terminal according to claim 154, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

160. (Previously Presented) A mobile information terminal according to claim 154, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

161. (Previously Presented) A mobile information terminal according to claim 154, wherein the memory transistor and the reference memory transistor store multilevel information.

162. (Previously Presented) A mobile information terminal comprising:

a display portion: and

a nonvolatile memory, the nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

a timer;

a first circuit for performing electrical write on the memory transistor for each time when an elapsed time measured by the timer reaches an arbitrarily preset time until a threshold voltage of the memory transistor, which is read based on a reference voltage of the reference memory transistor is higher than a first reference voltage; and

a second circuit for performing electrical write on the reference memory transistor until a threshold voltage of the reference memory transistor is higher than a second reference voltage.

163. (Previously Presented) A mobile information terminal according to claim 162, wherein the first reference voltage is higher than the second reference voltage.

164. (Previously Presented) A mobile information terminal according to claim 162, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

165. (Previously Presented) A mobile information terminal a according to claim 162, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

166. (Previously Presented) A mobile information terminal according to claim 162, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

167. (Previously Presented) A mobile information terminal according to claim 162, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

168. (Previously Presented) A mobile information terminal according to claim 162, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

169. (Previously Presented) A mobile information terminal according to claim 162, wherein the memory transistor and the reference memory transistor store multilevel information.

170. (New) A nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

a verify circuit;

a read circuit comprising a sense amplifier circuit having:

a first input terminal electrically connected to the memory transistor;

a second input terminal electrically connected to the reference memory transistor; and

an output terminal electrically connected to the verify circuit;

a first reference voltage supply electrically connected to the first input terminal and the second input terminal;

a second reference voltage supply electrically connected to the first input terminal and the second input terminal; and

a write circuit electrically connected to the verify circuit, the memory transistor and the reference memory transistor.

171. (New) A nonvolatile memory according to claim 170, wherein a voltage supplied by the first reference voltage supply is higher than a voltage supplied by the second reference voltage supply.

172. (New) A nonvolatile memory according to claim 170, wherein a voltage supplied by the second reference voltage supply is higher than a threshold voltage of the reference memory transistor.

173. (New) A nonvolatile memory according to claim 170, wherein the memory transistor and the reference memory transistor store multilevel information.

174. (New) A nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

a verify circuit;

a read circuit comprising:

a first bias circuit electrically connected to the memory transistor;

a second bias circuit electrically connected to the reference memory transistor;

a data latch circuit electrically connected to the verify circuit; and

a sense amplifier circuit having:

a first input terminal electrically connected to the first bias circuit;

a second input terminal electrically connected to the second bias circuit; and

an output terminal electrically connected to the latch circuit;

a first reference voltage supply electrically connected to the first input terminal and the second input terminal;

a second reference voltage supply electrically connected to the first input terminal and the second input terminal; and

a write circuit electrically connected to the verify circuit, the memory transistor and the reference memory transistor.

175. (New) A nonvolatile memory according to claim 174, wherein a voltage supplied by the first reference voltage supply is higher than a voltage supplied by the second reference voltage supply.

176. (New) A nonvolatile memory according to claim 174, wherein a voltage supplied by the second reference voltage supply is higher than a threshold voltage of the reference memory transistor.

177. (New) A nonvolatile memory according to claim 174, wherein the memory transistor and the reference memory transistor store multilevel information.

178. (New) A nonvolatile memory comprising:

a first power source;

a second power source;

a memory transistor electrically connected to the first power source;

a reference memory transistor electrically connected to the first power source;

a verify circuit;

a read circuit comprising:

a first resistance electrically connected between the memory transistor and the second power source;

a second resistance electrically connected between the reference memory transistor and the second power source;

a data latch circuit electrically connected to the verify circuit; and

a sense amplifier circuit having:

a first input terminal electrically connected to the memory transistor via a first switch;

a second input terminal electrically connected to the reference memory transistor via a second switch; and

an output terminal electrically connected to the latch circuit;

a first reference voltage supply electrically connected to the first input terminal via the first switch, and the second input terminal via the second switch;

a second reference voltage supply electrically connected to the first input terminal via the first switch, and the second input terminal via the second switch; and

a write circuit electrically connected to the verify circuit, the memory transistor and the reference memory transistor.

179. (New) A nonvolatile memory according to claim 178, wherein a voltage supplied by the first reference voltage supply is higher than a voltage supplied by the second reference voltage supply.

180. (New) A nonvolatile memory according to claim 178, wherein a voltage supplied by the second reference voltage supply is higher than a threshold voltage of the reference memory transistor.

181. (New) A nonvolatile memory according to claim 178, wherein the memory transistor and the reference memory transistor store multilevel information.